AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1-6. (Cancelled)

7. (Original) A method for designing an integrated circuit, comprising:

providing a first transistor in a first logic path, the first transistor having a first contact, a first gate length and a first contact to gate centerline spacing;

providing a second transistor in a second logic path, the second transistor having a second contact, a second gate length and a second contact to gate centerline spacing, the first contact to gate centerline spacing substantially equal to the second contact to gate centerline spacing; and

selecting a different gate length for the first gate length using a predetermined design criterion.

8. (Original) The method of Claim 7, wherein the first gate length and the second gate length are equal, and selecting a different gate length comprises selecting a different gate length without changing the placement of the first contact or the second contact.

9. (Original) The method of Claim 8, wherein providing a first transistor comprises providing a first cell comprising the first transistor and wherein selecting a different gate length comprises replacing the first cell with a substitute cell comprising a substitute transistor, the substitute transistor having a different gate length than the first gate length, the first cell and the substitute cell having the same footprint and operable to perform a same function.

10. (Original) The method of Claim 7, wherein the predetermined design criterion is based on the respective levels of leakage current of the first transistor and the second transistor.

11. (Original) The method of Claim 7, wherein the first logic path is a critical path and the different gate length is a gate length that is shorter than the first gate length.

12. (Original) The method of Claim 7, wherein the first logic path is a non-critical path and the different gate length is a gate length that is longer than the first gate length.

13. (Original) The method of Claim 7, wherein modeling a change of the gate length comprises changing the gate length by a length increment, the length increment less than the length of one grid of a design rule for the integrated circuit.

14-20. (Cancelled)